WHAT IS CLAIMED IS:

1. A system comprising:

a bus comprising signal lines; and

a device configured to be inserted onto and removed from the bus through contacts configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit.

2. The system of claim 1, where the pre-charge circuit comprises a resistor located between one of the contacts and the device.

3. The system of claim 1, comprising a switch located between the contacts and the device.

4. The system of claim 3, where the switch is a field effect transistor located between the contacts and the device.

5. The system of claim 3, where the switch is configured to conduct after the low-impedance is provided across the pre-charge circuit.

6. The system of claim 1, comprising reference contacts configured to provide a common reference to the bus and the device before contact between the pre-charge circuit and one of the signal lines as the device is inserted onto the bus.

7. The system of claim 1, comprising power contacts and reference contacts, where the reference contacts are configured to provide a common reference to the bus and the device before the power contacts provide power, and the power contacts provide power before contact between the pre-charge circuit and one of the signal lines as the device is inserted onto the bus.

8. The system of claim 1, comprising power contacts and reference contacts, where the power contacts provide power before the reference contacts provide a common reference to the bus and the device, and the reference contacts provide a common reference to the bus and the device before contact between the pre-charge circuit and one of the signal lines as the device is inserted onto the bus.

9. The system of claim 1, comprising power contacts, where the power contacts are configured to provide power at the same time as contact between the pre-charge circuit and one of the signal lines, as the device is inserted onto the bus.

10. The system of claim 1, where the signal lines comprise a serial data line and a serial clock line.

11. The system of claim 1, where the bus is an inter-integrated circuit bus.

12. A connector system, comprising:

a first connector; and

a second connector, where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line, and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system.

13. The connector system of claim 12, comprising:

a third connector; and

a fourth connector, where the third connector is configured to provide a second pre-charge circuit between the fourth connector and a second bus signal line, and the fourth connector is configured to provide a second short-circuit

between the fourth connector and the second bus signal line, where the third connector and the fourth connector are staggered to provide the second pre-charge circuit and the second short-circuit at different times during engagement and disengagement of the connector system.

14. The connector system of claim 13, where the first connector and the third connector are staggered to simultaneously provide the first pre-charge circuit between the second connector and the first bus signal line and the second pre-charge circuit between the fourth connector and the second bus signal line.

15. The connector system of claim 13, where the first connector and the third connector are staggered to provide the first pre-charge circuit between the second connector and the first bus signal line and the second pre-charge circuit between the fourth connector and the second bus signal line in a sequence.

16. The connector system of claim 13, where the second connector and the fourth connector are staggered to simultaneously provide the first short-circuit between the second connector and the first bus signal line, and the second short-circuit between the fourth connector and the second bus signal line.

17. The connector system of claim 13, where the second connector and the fourth connector are staggered to provide the first short-circuit between the second connector and the first bus signal line, and the second short-circuit between the fourth connector and the second bus signal line in a sequence.

18. A module connector, comprising:

a first contact configured to connect a resistive load to a signal line; and

a second contact configured to provide a low-impedance to the signal line and across the resistive load.

19. The module connector of claim 18, where the first contact and the second contact are on different pins of the module connector.

20. The module connector of claim 18, where the first contact and the second contact are on the same pin of the module connector.

21. An electronic system, comprising:

means for equalizing the voltage on a signal line with the voltage on a device contact while maintaining the voltage on the signal line; and

means for shorting the signal line to the device contact after the voltage on the signal line equals the voltage on the device contact.

22. The electronic system of claim 21, where the means for equalizing comprises a resistor coupled between the device contact and the signal line.

23. The electronic system of claim 21, where the means for equalizing is in a parallel circuit configuration with the means for shorting after the device contact is shorted to the signal line.

24. The electronic system of claim 21, where the means for equalizing comprises a first connection and the means for shorting comprises a second connection configured to be staggered from the first connection to complete the first connection before completing the second connection as the signal line is coupled to the device contact.

25. The electronic system of claim 21, comprising means for buffering a device from the signal line before the voltage on the signal line equals the voltage on the device contact.

26. A method for hot coupling a device to a bus, comprising:

equalizing voltages on device contacts and corresponding bus signal lines;

maintaining the voltages on the corresponding bus signal lines as the voltages on the device contacts and the corresponding bus signal lines are equalized; and

connecting the device contacts to the corresponding bus signal lines.

27. The method of claim 26, comprising:

electrically coupling a device power line to a bus power line prior to equalizing voltages.

28. The method of claim 26, comprising:

electrically coupling a device reference line to a bus reference line prior to equalizing voltages.

29. The method of claim 28, where equalizing voltages and maintaining the voltages comprises:

electrically coupling a serial data line of the bus to one of the device contacts through a data line resistor; and

electrically coupling a serial clock line of the bus to another one of the device contacts through a clock line resistor.

30. The method of claim 29, comprising:

providing a data line switch;

providing a clock line switch;

activating the data line switch; and

activating the clock line switch.